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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/023,147	12/18/2001	Kohji Takano	JP9-2000-0304-US1	3176

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EXAMINER	
LABAZE, EDWYN	
ART UNIT	**PAPER NUMBER**
2876	

DATE MAILED: 02/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/023,147	TAKANO ET AL.	
	Examiner	Art Unit	
	EDWYN LABAZE	2876	

-- Th MAILING DATE of this c mmunication app ars on the cov r sh t with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 December 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 December 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Receipt is acknowledged of IDS filed on 18/18/2001.

2. Receipt is acknowledged of Change of address filed on 11/8/2002.

3. Claims 1-16 are presented for examination.

Priority

4. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Drawings

5. Figure 7 is disclosed by the applicant (page 11, line 12) in the background and should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-16 are rejected under 35 U.S.C. 102(b) as being unpatented by Pfeiffer et al. (U.S. 4,955,024).

Re claims 1 and 9: Pfeiffer et al. discloses a system, which includes a plural of registers (col.5, line 23); an arithmetic unit 146 (col.14, line 31); and a plurality of memories, wherein

reading of multiple variables from the plurality of memories to the plurality of registers is performed during the same reading cycle by way of a pipeline process 136 performed by the arithmetic unit 148 (col.17, lines 1-68 and col.18, lines 1-35), also means of performing an arithmetic operation (col.14, lines 62-67), means of writing the results in input registers (col.14, lines 21-30), and reading multiple variables X and Y from the memories and storing the variables in multiple registers during the pipeline stage (col.14, lines 13-21).

Re claims 2 and 10: Pfeiffer et al. teaches a system, wherein the arithmetic unit 146 is a multiplier adder 150 (col.15, line 18) for, based on values X1, X2, X3, and X4 having an r-bit length that are respectively input to a first register, second register, third register, and fourth register, or a four-port register 144 providing a result Q for X1+X2+X3+X4 having a length of 2r bits or 2r+1 bits (col.16, lines 5-60).

Re claims 3 and 11: Pfeiffer et al. discloses a system, wherein the multiple memories include a first 82 and a second memory 226 (col.20, lines 43-46); and wherein, at a stage for writing an operation result, which follows the operation stage of the pipeline process, lower r bits Ql of the operation result Q are recorded in the first memory and upper bits Qh of the operation result Q, excluding the bits Ql are recorded in the fourth register 144 (col.18, lines 57-67 and col.19, lines 43-55) while at a stage for reading variables from the registers, which follows the writing stage, simultaneously, a variable X1 is read from the first memory and is stored in the first register, and a variable X3 is read from the second memory and stored in the third register 260 (col.24, lines 3-35).

Re claims 4 and 12: Pfeiffer et al. teaches a system, wherein the first memory and second memory are two-port memories having one data writing port and data reading port (col.11, lines 41-53).

Re claims 5 and 13: Pfeiffer teaches a system, wherein the first memory 82 is a two-port memory having one data writing port and one data reading port (col. col.11, lines 41-53), while the second memory is a single-port memory 464 having one port for the writing and data reading (col.38, lines 61-68 and col.39, lines 1-68).

Re claims 6 and 14: Pfeiffer et al. teaches a system, wherein the arithmetic unit 148 is a multiplier adder 150 (col.15, line 18) for, based on values X1, X2, X3, X4, X5 and X6 having an r-bit length (see table VI, col. 87, 88) that are respectively input to a first register, second register, third register, a fourth register, a fifth register, and a sixth register providing a result Q for X1+ X2 + X3 + X4 + X6 + X6, which have a length of 2r bits or 2r+1 bits (col.17, lines 43-52 and col.60, lines17-67).

Re claims 7 and 15: Pfeiffer et al. discloses a system, wherein the multiple memories include a first 82 and a second memory 226 (col.20, lines 43-46) and a third memory (col.); and wherein, at a stage for writing an operation result, which follows the operation stage of the pipeline process, lower r bits Ql of the operation result Q are recorded in the first memory and upper bits Qh of the operation result Q, separately or excluding the bits Ql are recorded in the sixth register (col.63, lines 10-25) while at a stage for reading variables from the registers, which follows the writing stage, simultaneously, a variable X3 is read from the first memory and is stored in the third register 627, and a variable X5 is read from the third memory and stored in the fifth register 629 (col.62, lines 1-35).

Re claims 8 and 16: Pfeiffer teaches a system, wherein the first memory 82 is a two-port memory having one data writing port and one data reading port (col. col.11, lines 41-53), while the second memory is a single-port memory 464 having one port for the writing and data reading (col.38, lines 61-68 and col.39, lines 1-68).

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Iwase et al. (U.S. 6,052,705) discloses a video signal processor with triple port memory.

Vassar (U.S. 4,488,252) teaches floating-point addition architecture.

Pfeiffer et al. (U.S. 5,146,592) discloses high-speed image processing computer with overlapping windows-Div.

Taddei (U.S. 3,689,983) teaches an accounting machine processor.

Rikuma (U.S. 4,827,113) discloses a technique for authenticating IC card and terminal.

Pfeiffer et al. (U.S. 4,985,848) teaches a high speed image processing system using separate data processor and address generator.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to EDWYN LABAZE whose telephone number is (703) 305-5437. The examiner can normally be reached on 7:30 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael G. Lee can be reached on (703) 305-3503. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-1782.

el
Edwyn Labaze
Patent Examiner
Art Unit 2876
February 4, 2003

KARL D. FRECH
PRIMARY EXAMINER